Customer No.:31561
Application No.: 10/709,767
Docket No.: 13292-US-PA

REMARKS

Present Status of the Application

Claims 1-7 are elected while claims 8-16 are withdrawn and claims 17-20 are cancelled. Claims 17-20 are reserved in right for applying Divisional Application later.

Applicants appreciate that claims 5-7 are considered being patentable.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Torgerson et al. (U. S. Patent 6,481,817; hereinafter Torgerson). Applicant has amended specification to correct typo errors. Applicants have amended independent claim 1 in combination with claim 3 while original claim 3 being currently cancelled. After entry of amendments, claims 1-2 and 4-7 remain pending in the present application, and reconsideration of those claims is respectfully requested.

About amendments

Applicants have amended "buffer signal" into "switching signal". These amendments can be clearly supported in FIG. 3 without adding new matter.

Discussion of Office Action Rejections

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Torgerson. Applicants respectfully traverse the rejections for at least the reasons set forth below. Applicant have amended independent claim 1.

1. As shown in FIG. 3 of the preferable embodiment of the present invention, the circuit

301, for example, receives an address signal A1 and a selection signal SEL. In the present invention, the circuit 301 includes several inverters, which are under control by the same address signal.

Further as recited in amended claim 1, it should be noted that the printhead controller in the present invention is implemented within the printhead, not on the printer portion as referred (as the print control device 36 of Torgerson) by the Office Action.

Basically, as can be understood, the selection signal is used to select a desired printhead control unit, for example, the black printhead or color printhead, to work. The address signal is used to enable the desired ink jetting circuit. The final output signal is determined from the logic voltage levels of the selection signal and the address signal.

2. In re Torgerson, the circuit of Fig. 6 is referred by the Office Action to provide the buffer circuit. However, Applicants respectfully disagree.

First, the Office Action refers to print control device 36 of Torgerson as the printhead controller of the present invention. However, ***print control device 36 of Torgerson is belonging to the printer portion but not in the printhead 24***.

Further, in Fig. 6 of Torgerson, ***it should be noted the MOS transistors 50 and 52 are switching devices but not the inverters, respectively***. The enable signals E(1) and E(2) are considered by the Office Action as the selection signals to control the switching devices 50 and 52.

Usually, when the switching device 50 is enabled by the enable signal E(1), the address

signal A(1) *is immediately passed* and enables the switching device 48 (col. 7, line 62 - col. 8, line 8). *In other words, for the person having the ordinary skill in the art, it is apparent that the switching device 50 of Torgerson does not serve as an inverter*. In short, when the switching device 50 is on (enabled), *the output signal outputs from the source terminal of the switching devices 50 corresponding to the address signal*. *The logic level of the input (drain) of the switching device is the same as that of the output (source) when the switching device is enabled*. On the contrary, taking Fig.4 of one of embodiments of the present application for example, if SEL and A1 are logic high, *the logic level of the input of the inverter 305A (SEL) is opposite to that of the output (the signal that flows to F2), and the logic level of the input of the inverter 307A (the signal flowing into F2) is opposite to that of the output (switching signal)*. Therefore, *the switching devices 50 and 52 are not the inverters* in circuit 301 of the present invention.

Also, when the switching device 48 is active (while the switching device 50 is enabled by E(1)), the switching device 52, under control by E(2), should be inactive (col. 8, lines 22-27). Oppositely, when the switching device 48 is inactive (switching device 50 is inactive) then the switching device 52 should be active (col. 8, lines 28-47; particularly to lines 44-47). As clearly seen in FIG. 8 of Torgerson, *only one of the enable signals E(1) and E(2) can be at high logic level, so as to for sure one of switching device 50 and 52 is "ON" while the other one is "OFF". The enable signals E(1) and E(2) CANNOT and SHOULD NOT be at high logic level at the same time period, as apparently shown in Figs. 8 and 9 of Torgerson.* The operation principle of the embodiments of the present application is totally different from that in

Torgerson, in which the *multiple inverters of the present application (as explicitly explained in the above)*, not the simple switching devices like those in Torgerson (switching devices 50 and 52), constitute a circuit for receiving the corresponding address signal and selection signal to obtain the switching signal, based on the logic level of the address signal and selection signal, to enable a specified jetting circuit. ***For a specified jetting circuit to be enabled in the present application, the corresponding address signal and selection signal, as shown in Fig. 4 for example, are both at high logic level.***

For at least the foregoing reasons, Applicants respectfully submit that independent claim 1 patently defines over the prior art, and should be allowed. For at least the same reasons, dependent claims 2 and 4-7 patently define over the prior art references as well. Wherein, claims 5-7 have been considered to be allowable.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-2 and 4-7 of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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